Q.P. Code: **16EC424** **R16**

Reg. No: | | | | | | | | | | |

SIDDHARTH INSTITUTE OF ENGINEERING & TECHNOLOGY:: PUTTUR

(AUTONOMOUS)

B.Tech III Year II Semester Supplementary Examinations March-2021

DIGITAL IC APPLICATIONS

(Electronics and Communication Engineering)

Time: 3 hours Max. Marks: 60

(Answer all Five Units **5 x 12 = 60** Marks)

UNIT-I

1	a	Draw the circuit diagram of basic CMOS gate and explain its operation.	6M
	b	Compare CMOS, TTL and ECL logic families.	6M
		OR	
2	a	Design a 4-input CMOS AND-OR-INVERTER gate. Draw the logic diagram and functional table.	6M
	b	Explain the following terms with reference to TTL gate i) D.C noise margin ii) Logic levels	6M

UNIT-II

3	a	Explain the various data types supported by VHDL. Give the necessary examples.	6M
	b	Explain about VHDL program structure.	6M
		OR	
4	a	Write about structural design elements with an example.	6M
	b	Write a VHDL entity and Architecture for the following function. F(x) = (a + b) (c d) Also draw the relevant logic diagram.	6M

UNIT-III

5	a	Design a 4 to 16 decoder with 74×138 IC's.	6M
	b	Write a VHDL program for the above design.	6M
		OR	
6	a	Design a priority encoder that can handle 32 requests. Use 74×148 and required discrete gates. Provide the truth table and explain the operation.	8M
	b	Draw the logic symbol of 74 x 85, 4-bit comparator.	4M

UNIT-IV

7	a	Design an 8 bit parallel in and serial out shift register and explain its operation with th timing waveforms.	8M
	b	Draw the logic diagram of IC 74194.	4M
		OR	
8	a	Design a bit LFSR counter using 74x194.List out the sequence assuming that the initial state 111.	6M
	b	Write a VHDL code for the LFSR counter using 74x194.	6M

UNIT-V

9	a	Design a 8-bit barrel shifter using three control inputs.	6M
	b	Write a VHDL program for the same in data flow style.	6M
		OR	
10	a	Distinguish between latch and flip flop .Show the logic diagram for both.	6M
	b	Explain the operation with the help of function table for latch and flip flop.	6M

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